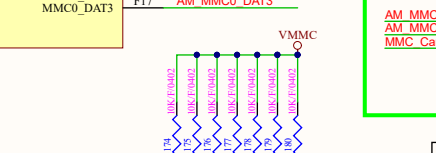
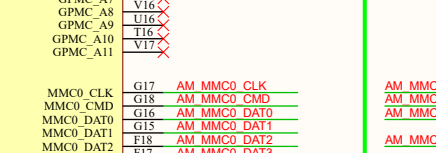
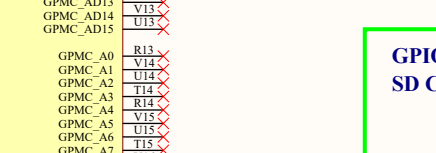
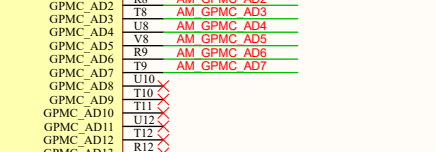
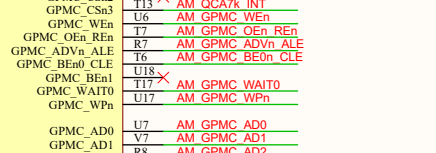
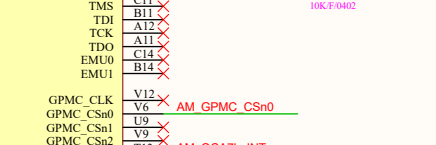
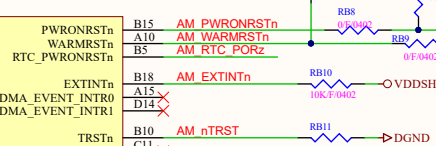
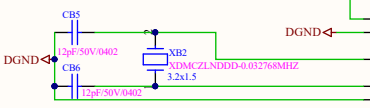
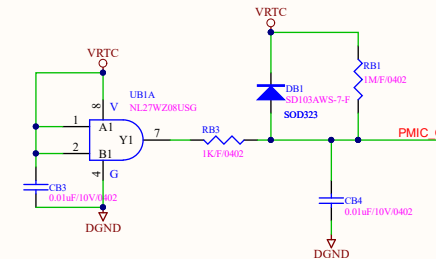
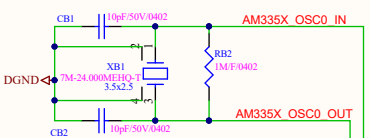


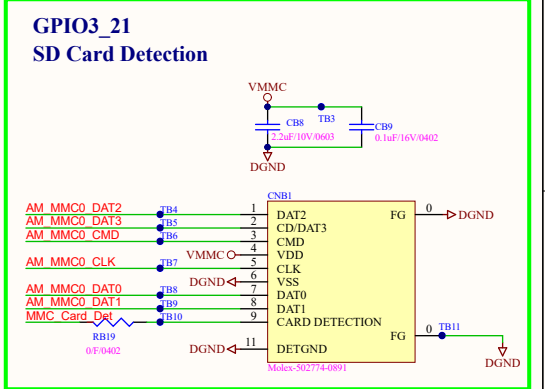
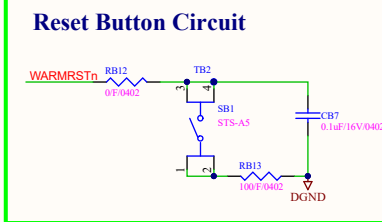
# System clock



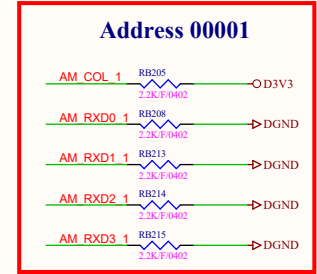
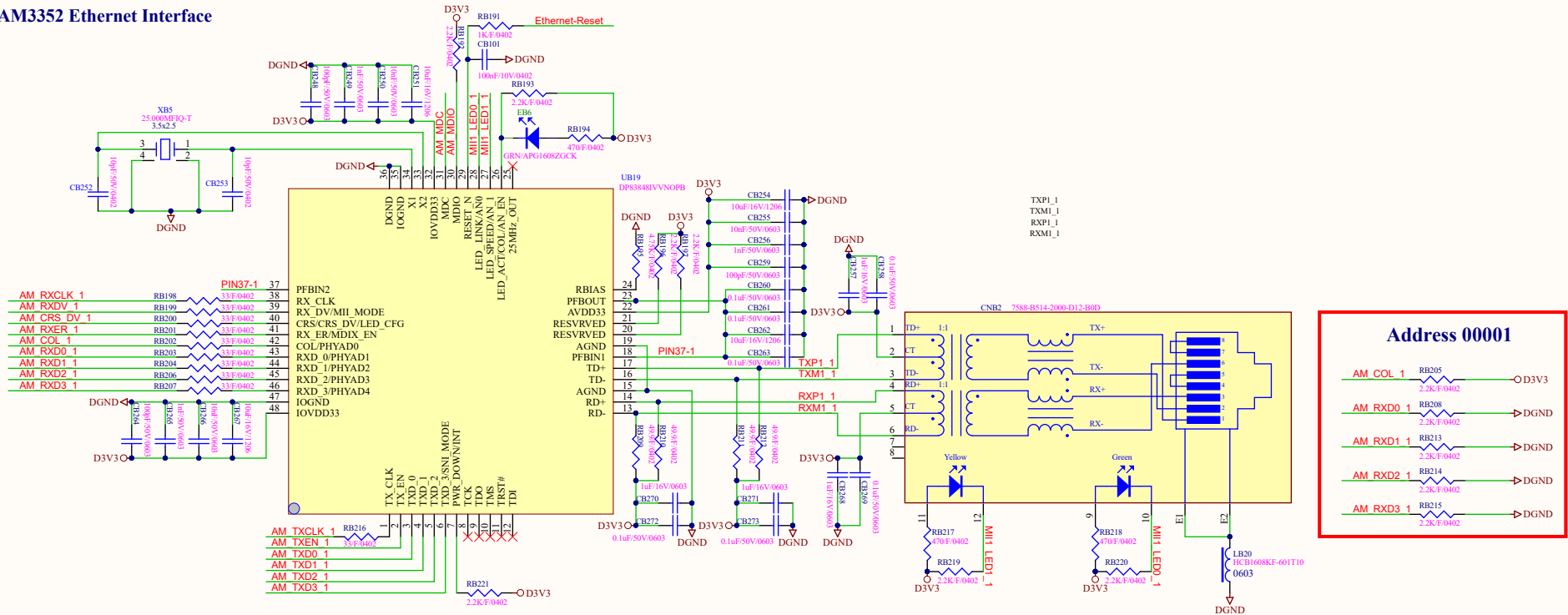
Differential impedance(100Ω)  
AM\_DDR\_CK  
AM\_DDR\_CkIn

## Group3

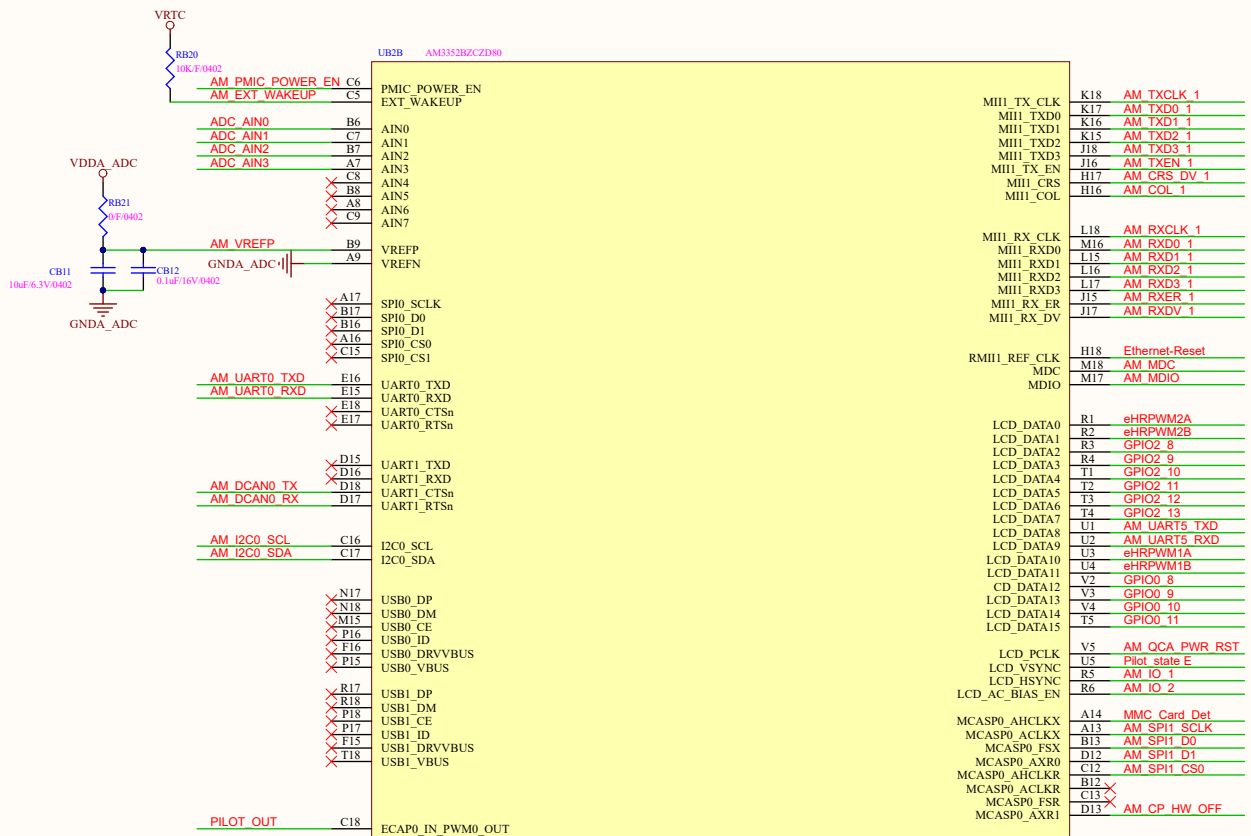
AM_DDR_A0	F3	DDR_A0
AM_DDR_A1	H1	DDR_A1
AM_DDR_A2	F4	DDR_A2
AM_DDR_A3	C3	DDR_A3
AM_DDR_A4	C2	DDR_A4
AM_DDR_A5	B1	DDR_A5
AM_DDR_A6	D5	DDR_A6
AM_DDR_A7	E2	DDR_A7
AM_DDR_A8	D4	DDR_A8
AM_DDR_A9	C1	DDR_A9
AM_DDR_A10	F4	DDR_A10
AM_DDR_A11	F2	DDR_A11
AM_DDR_A12	E3	DDR_A12
AM_DDR_A13	H3	DDR_A13
AM_DDR_A14	H4	DDR_A14
AM_DDR_A15	D3	DDR_A15
AM_DDR_BA0	C4	DDR_BA0
AM_DDR_BA1	E1	DDR_BA1
AM_DDR_BA2	B3	DDR_BA2
AM_DDR_A9		
AM_DDR_A10	M3	DDR_D0
AM_DDR_A11	H1	DDR_D1
AM_DDR_A12	N1	DDR_D2
AM_DDR_A13	N2	DDR_D3
AM_DDR_A14	N3	DDR_D4
AM_DDR_BA0	N4	DDR_D5
AM_DDR_BA1	P3	DDR_D6
AM_DDR_BA2	P4	DDR_D7
AM_DDR_CKE	J1	DDR_D8
AM_DDR_CSn0	K1	DDR_D9
AM_DDR_CASn	K2	DDR_D10
AM_DDR_RASn	K3	DDR_D11
AM_DDR_WEEn	K4	DDR_D12
AM_DDR_ODT	L3	DDR_D13
AM_DDR_RESEtIn	L4	DDR_D14
AM_DDR_RESEtIn	M1	DDR_D15
AM_DDR_CK	D2	DDR_CK
AM_DDR_CkIn	D1	DDR_CKIn
AM_DDR_CKE	G3	DDR_CKIn
AM_DDR_CSn0	H2	DDR_CSn0
AM_DDR_CASn	F1	DDR_CASn
AM_DDR_RASn	G4	DDR_RASn
AM_DDR_WEEn	B2	DDR_WEEn
AM_DDR_DQM0	M2	DDR_DQM0
AM_DDR_DQS0	P1	DDR_DQS0
AM_DDR_DQS0n0	P2	DDR_DQS0n0
AM_DDR_DQM1	J2	DDR_DQM1
AM_DDR_DQS1	L1	DDR_DQS1
AM_DDR_DQS1n1	L2	DDR_DQS1n1
AM_DDR_ODT	G1	DDR_ODT
AM_DDR_RESEtIn	G2	DDR_RESEtIn
AM_DDR_VTP	J3	DDR_VTP
AM_DDR_VREF	J4	DDR_VREF



# AM3352 Ethernet Interface



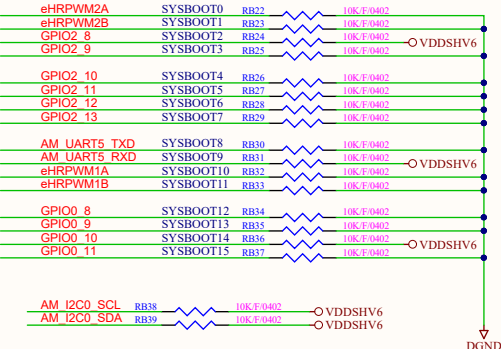
<b>PHIHONG TECHNOLOGY CO.,LTD</b>			
Title <b>CCS-00-R(Ethernet interface)_5.0.SchDoc</b>			
Size <b>A3</b>	Document Number	Rev	
Date <b>2019/12/16</b>	ya fen	Sheet	1 of 11



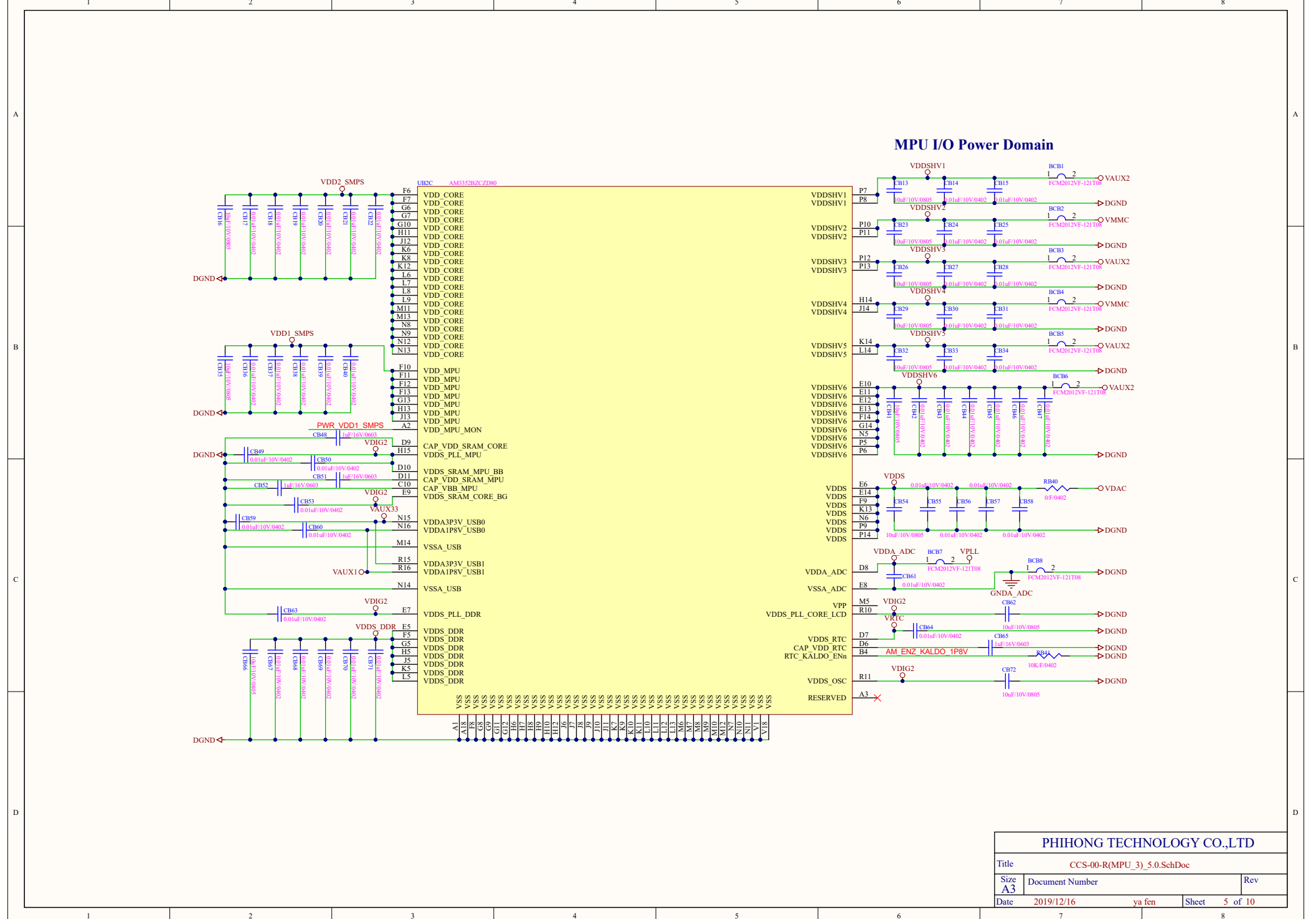
**Boot Sequence UART MMC0 NAND**

**SYSBOOT[0:15] = 0010 0000 0000 0010**

**BOOT Configuration**



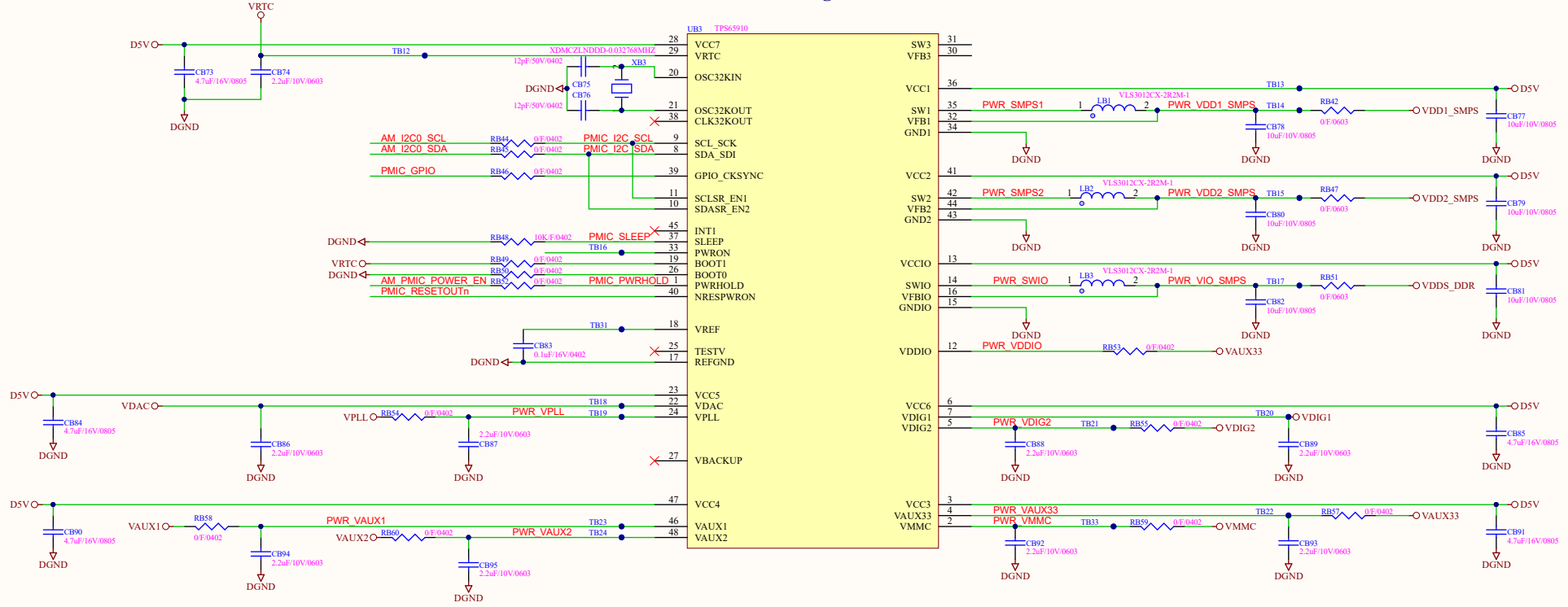
<b>PHIHONG TECHNOLOGY CO.,LTD</b>		
Title <b>CCS-00-R(MPU_2)_5.0.SchDoc</b>		
Size <b>A3</b>	Document Number	Rev
Date <b>2019/12/16</b>	ya fen	Sheet <b>4 of 10</b>



<b>PHIHONG TECHNOLOGY CO.,LTD</b>		
Title <b>CCS-00-R(MPU_3)_5.0.SchDoc</b>		
Size <b>A3</b>	Document Number	Rev
Date <b>2019/12/16</b>	ya fen	Sheet <b>5</b> of <b>10</b>

# Power Management IC

UB3 TPS6910



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Title			CCS-00-R(Power IC)_5.0.SchDoc		
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Group1

Group2

AM\_DDR\_DQS0  
AM\_DDR\_DQSn0

AM\_DDR\_DQS1  
AM\_DDR\_DQSn1

AM\_DDR\_D0  
AM\_DDR\_D1  
AM\_DDR\_D2  
AM\_DDR\_D3  
AM\_DDR\_D4  
AM\_DDR\_D5  
AM\_DDR\_D6  
AM\_DDR\_D7  
AM\_DDR\_DQM0

AM\_DDR\_D8  
AM\_DDR\_D9  
AM\_DDR\_D10  
AM\_DDR\_D11  
AM\_DDR\_D12  
AM\_DDR\_D13  
AM\_DDR\_D14  
AM\_DDR\_D15  
AM\_DDR\_DQM1

AM\_DDR\_RESEtN T2  
AM\_DDR\_CK J7  
AM\_DDR\_CkN K7  
AM\_DDR\_CKE K9  
AM\_DDR\_CSn0 L2  
AM\_DDR\_RASn L3  
AM\_DDR\_CASn K3  
AM\_DDR\_WEN L3

AM\_DDR\_D0 E3  
AM\_DDR\_D1 F7  
AM\_DDR\_D2 F2  
AM\_DDR\_D3 F8  
AM\_DDR\_D4 H3  
AM\_DDR\_D5 H8  
AM\_DDR\_D6 G2  
AM\_DDR\_D7 H7  
AM\_DDR\_D8 D7  
AM\_DDR\_D9 C3  
AM\_DDR\_D10 C8  
AM\_DDR\_D11 C2  
AM\_DDR\_D12 A7  
AM\_DDR\_D13 A2  
AM\_DDR\_D14 B8  
AM\_DDR\_D15 A3

AM\_DDR\_DQS1 C7  
AM\_DDR\_DQSn1 B7  
AM\_DDR\_DQM1 D3  
AM\_DDR\_DQSn0 G3  
AM\_DDR\_DQS0 F3  
AM\_DDR\_DQM0 E7

NCJ1  
NCJ9  
L1  
L9  
M7

B2  
D9  
G7  
K2  
K8  
N1  
N9  
R1  
R9

RESEtN  
CK  
CKn  
CKE  
CSn  
RASn  
CASn  
WEN

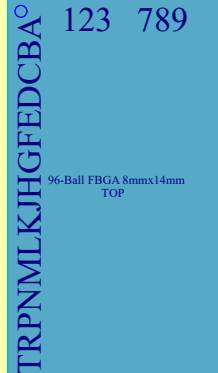
DO0  
DO1  
DO2  
DO3  
DO4  
DO5  
DO6  
DO7  
DO8  
DO9  
DO10  
DO11  
DO12  
DO13  
DO14  
DO15

UDQS  
UDQSn  
UDM  
LDQSn  
LDQS  
LDM

VDD  
VDD  
VDD  
VDD  
VDD  
VDD  
VDD  
VDD  
VDD  
VDD

VSS  
VSS  
VSS  
VSS  
VSS  
VSS  
VSS  
VSS  
VSS  
VSS

MT41K256M16TW-107 IT:P



96-Ball FBGA 8mmx14mm  
TOP

A0  
A1  
A2  
A3  
A4  
A5  
A6  
A7  
A8  
A9  
A10  
A11  
A12  
A13  
A14

BA0  
BA1  
BA2

ODT  
K1

VREFCA  
M8

VREFDQ  
H1

ZQ  
L8

VDDQ  
A1  
VDDQ  
A8  
VDDQ  
C1  
VDDQ  
C2  
VDDQ  
D2  
VDDQ  
E9  
VDDQ  
F1  
VDDQ  
H2  
VDDQ  
H9

VSSQ  
G9  
VSSQ  
G4  
VSSQ  
E8  
VSSQ  
E2  
VSSQ  
D8  
VSSQ  
D1  
VSSQ  
B9  
VSSQ  
B1

N3  
P7  
P3  
N2  
P8  
P2  
R8  
R2  
T8  
R3  
L7  
R7  
N7  
T3  
T7

M2  
N8  
M3

DDR ODT  
Rb65  
Q1F0402  
AM\_DDR\_ODT

AM\_DDR\_VREF

DDR VREFDQ  
Rb66  
Q2F0402  
AM\_DDR\_VREF

DGND

VDDSDR  
Rb67  
Q20F0402

DGND

UB8

NC  
NC  
NC  
NC  
NC  
R/B2#  
R/B#  
RE#  
CE#  
CE2#  
NC  
VCC  
VSS  
NC  
NC  
NC  
NC  
ALE  
WE#  
WP#  
NC  
NC  
NC  
NC  
NC

MT29F16G08ABACAW-ITZ-C  
TSOP(48)  
20mm x 12mm  
Asynchronous Only

DNU/VSSQ  
NC  
NC  
NC  
NC  
NC  
DO7  
DO6  
DO5  
DO4  
DO3  
DO2  
DO1  
DO0  
NC  
NC  
NC  
NC  
DNU/VCCQ  
DNU/VCC  
VCC  
VSS  
DNU  
DNU  
NC  
NC  
DO3  
DO2  
DO1  
DO0  
NC  
NC  
DNU  
DNU/VSSQ

DGND  
AM\_GPMC\_AD7  
AM\_GPMC\_AD6  
AM\_GPMC\_AD5  
AM\_GPMC\_AD4  
AM\_GPMC\_AD3  
AM\_GPMC\_AD2  
AM\_GPMC\_AD1  
AM\_GPMC\_AD0

VAUX33  
CB115  
CB114  
CB113  
CB112  
CB111  
CB110

DGND

AM\_GPMC\_WAIT0  
AM\_GPMC\_OEn\_REn  
AM\_GPMC\_CSn0  
AM\_GPMC\_BE0n\_CLE  
AM\_GPMC\_ADVn\_ALE  
AM\_GPMC\_WEn  
AM\_GPMC\_WPn

AM\_GPMC\_AD0  
AM\_GPMC\_AD1  
AM\_GPMC\_AD2  
AM\_GPMC\_AD3  
AM\_GPMC\_AD4  
AM\_GPMC\_AD5  
AM\_GPMC\_AD6  
AM\_GPMC\_AD7

VAUX33  
Rb68  
10K-F0402  
AM\_GPMC\_WAIT0  
VAUX33  
Rb69  
10K-F0402  
AM\_GPMC\_OEn\_REn  
CB119  
0.1uF16V/0402  
DGND  
VAUX33  
Rb75  
10K-F0402  
AM\_GPMC\_CSn0

AM\_GPMC\_WAIT0  
AM\_GPMC\_OEn\_REn  
AM\_GPMC\_CSn0  
AM\_GPMC\_BE0n\_CLE  
AM\_GPMC\_ADVn\_ALE  
AM\_GPMC\_WEn  
AM\_GPMC\_WPn

AM\_GPMC\_AD7 Rb70 10K-F0402 VAUX33  
AM\_GPMC\_AD6 Rb71 10K-F0402 VAUX33  
AM\_GPMC\_AD5 Rb72 10K-F0402 VAUX33  
AM\_GPMC\_AD4 Rb73 10K-F0402 VAUX33  
AM\_GPMC\_AD3 Rb74 10K-F0402 VAUX33  
AM\_GPMC\_AD2 Rb76 10K-F0402 VAUX33  
AM\_GPMC\_AD1 Rb77 10K-F0402 VAUX33  
AM\_GPMC\_AD0 Rb78 10K-F0402 VAUX33

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Table with 4 columns: Title, Size, Date, and Sheet/Rev info.

A

B

C

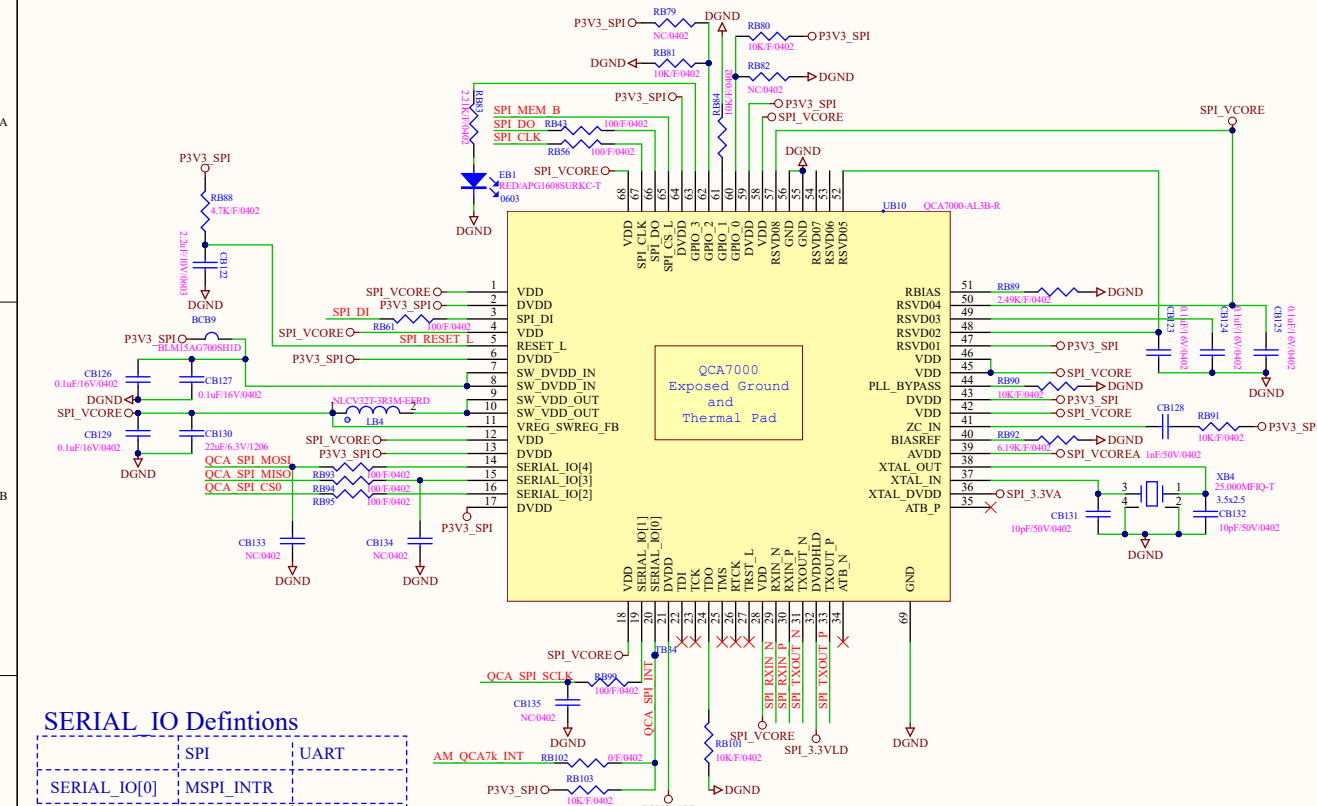
D

A

B

C

D



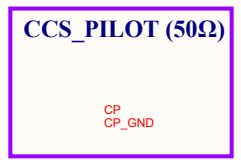
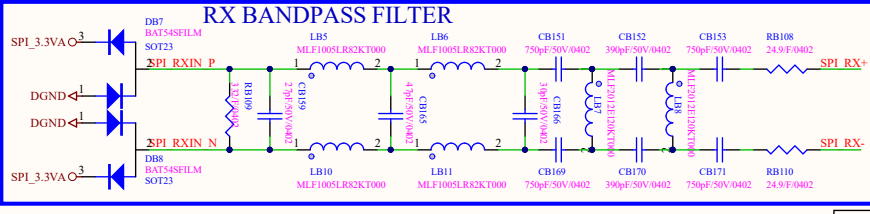
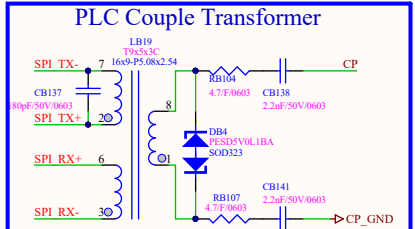
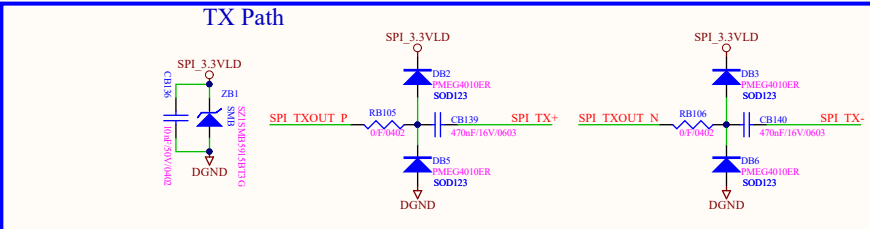
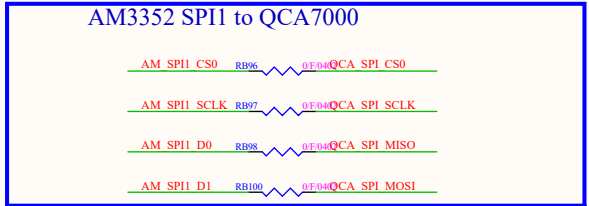
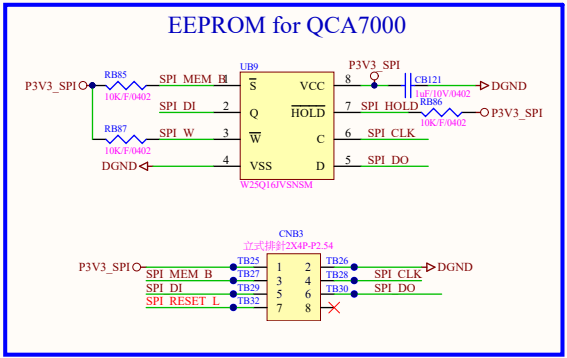
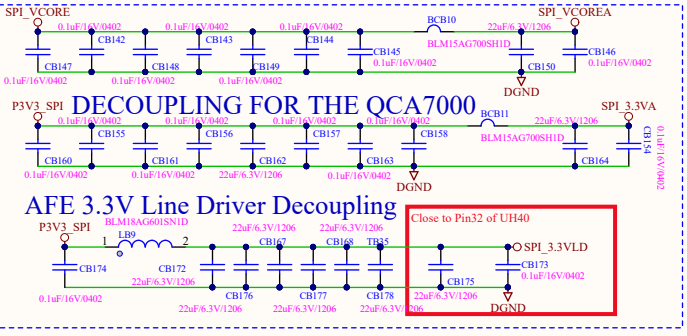
QCA7000  
Exposed Ground  
and  
Thermal Pad

GPI02\_0 for QCA7K SPI1 interrupt

### SERIAL\_IO Defintions

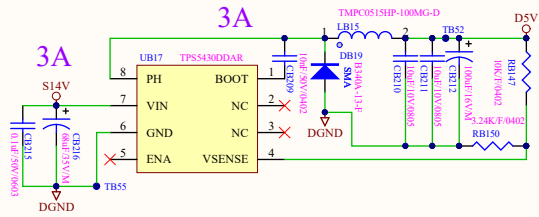
	SPI	UART
SERIAL_IO[0]	MSPI_INTR	
SERIAL_IO[1]	MSPI_CLK	UART RTS
SERIAL_IO[2]	MSPI_CS	UART_CTS
SERIAL_IO[3]	MSPI_MISO	UART_TXD
SERIAL_IO[4]	MSPI_MOSI	UART_RXD

NOTE : Place these capacitors as close to power pins in the QCA7000 as possible.



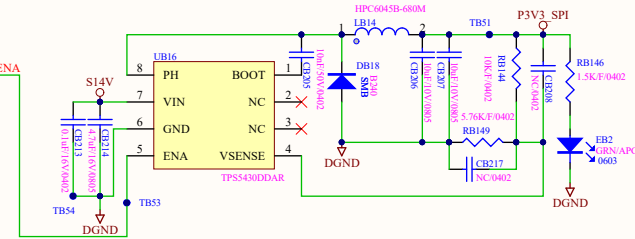
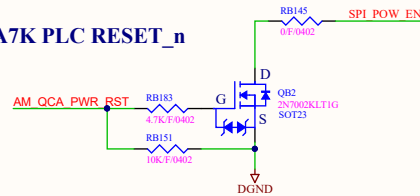
PHIHONG TECHNOLOGY CO.,LTD			
Title	CCS-00-R(PLC)_5.0.SchDoc		
Size	Document Number		Rev
Date	2019/12/16	ya fen	Sheet 6 of 10

### S14V to D5V Buck for PMIC



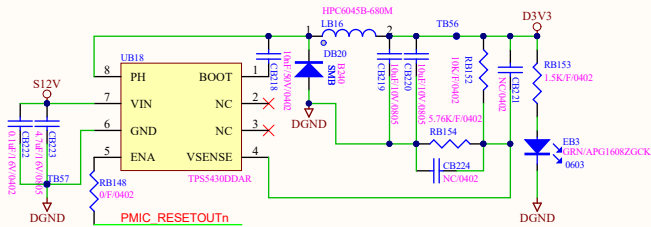
$$D5V = V_{ref} \times (1 + RH30/RH32) = 1.221 \times (1 + 10/3.24) = 4.99$$

### QCA7K PLC RESET\_n



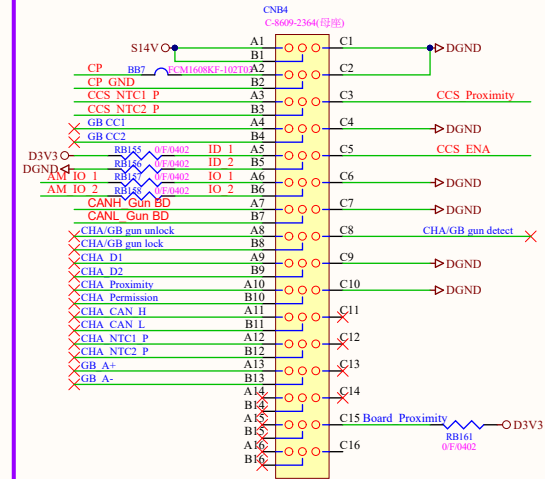
$$P3V3 = V_{ref} \times (1 + RH46/RH49) = 1.221 \times (1 + 10/5.76) = 3.34$$

### S12V to D3V3

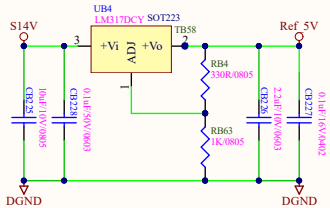


$$P3V3 = V_{ref} \times (1 + RH46/RH49) = 1.221 \times (1 + 10/5.76) = 3.34$$

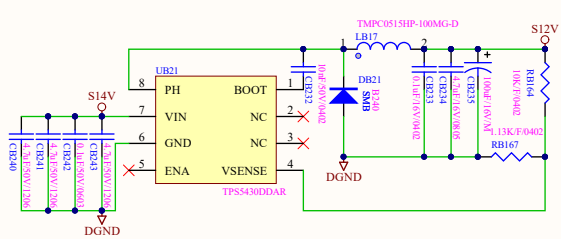
### Interface for Communication Board



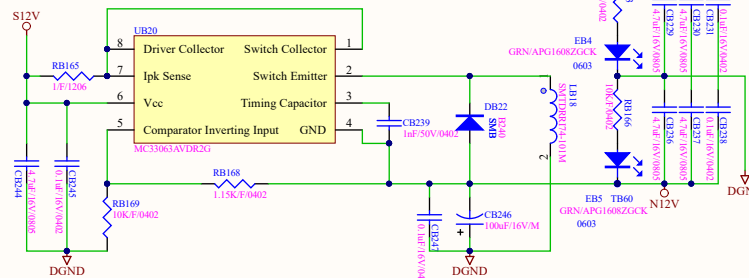
### S14V to Ref\_5V LDO for Control Pilot Offset circuit



### PE\_P12V /PE\_N12V Power for control pilot circuit



$$PE\_P12V = V_{ref} \times (1 + RH353/RH354) = 1.221 \times (1 + 10/1.13) = 12.03$$



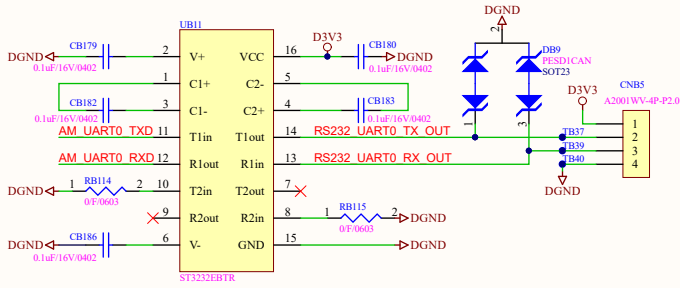
$$PE\_N12V = V_{ref} \times (1 + RH48/RH45) = 1.25 \times (1 + 10/1.15) = 12.12$$

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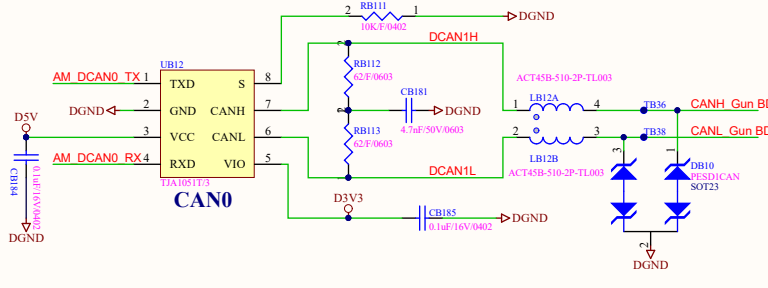
Title			CCS-00-R(Power Back+Connector)_5.0.SchDoc
Size	Document Number	Rev	
A3			
Date	2019/12/16	ya fen	Sheet 10 of 10



### RS232(UART0-Debug/UART2-RFID)



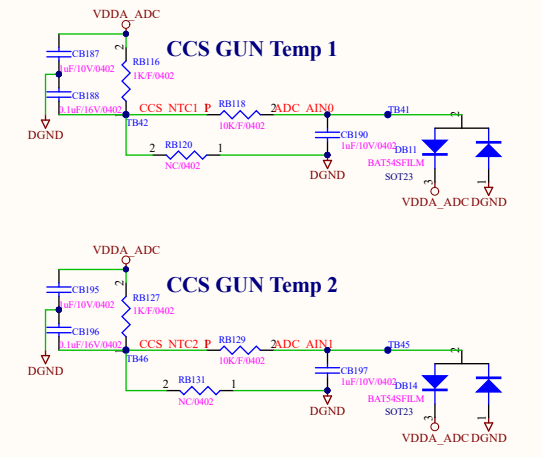
### CAN0 for Communication Board



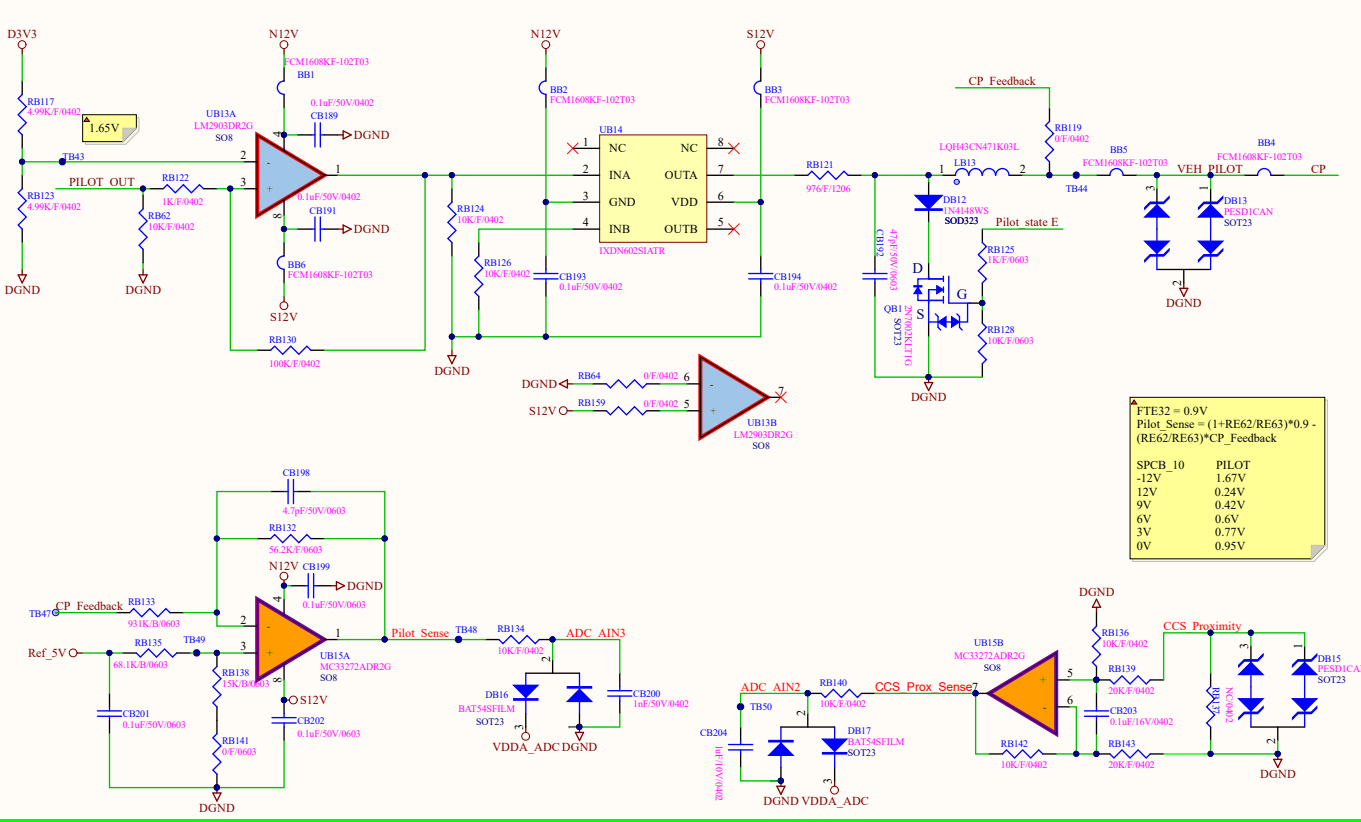
**CAN BUS (120Ω)**

DCAN1H  
DCAN1L  
CANH\_Gun BD  
CANL\_Gun BD

### GUN



### Control Pilot

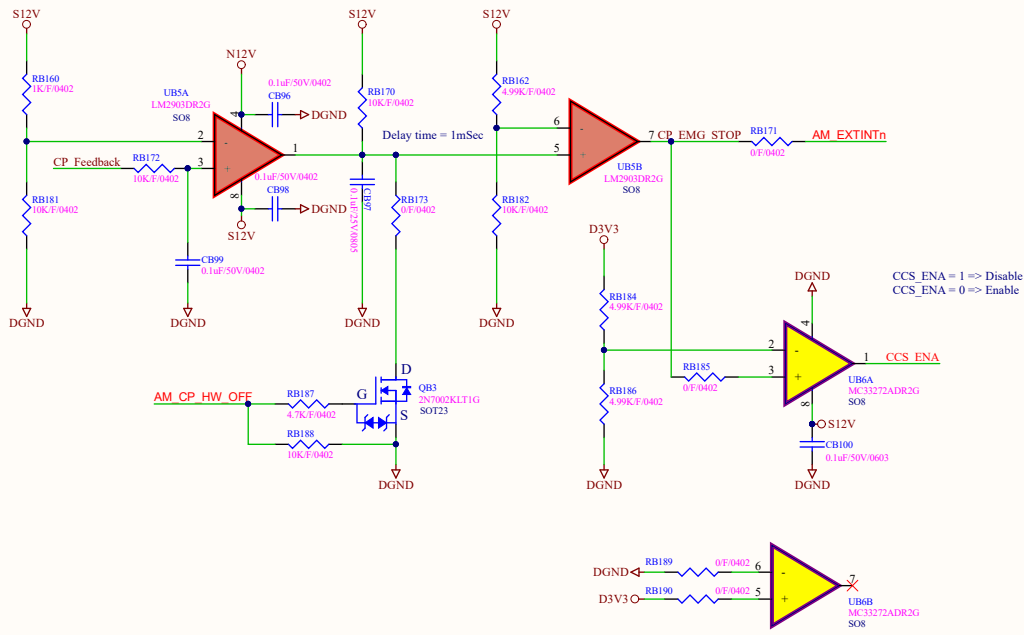


$V_{TE32} = 0.9V$   
 $Pilot\_Sense = (1 + RE62/RE63) * 0.9 - (RE62/RE63) * CP\_Feedback$

SPCB_10	PILOT
-12V	1.67V
12V	0.24V
9V	0.42V
6V	0.6V
3V	0.77V
0V	0.95V

AIN2  
 CCS GUN Proximity Detection  
 AIN2=CCS\_Proximity/2

PHIHONG TECHNOLOGY CO.,LTD			
Title CCS-00-R(RS+GUN+CAN+Pilot)_5.0.schdoc			
Size A3	Document Number		Rev 1.0
Date 2019/12/16	ya fen	Sheet 9	of 10



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Title			CCS-00-R(CP HW detection)_5.0.schdoc		
Size	Document Number				Rev
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